Abstract

A feed forward equalizer for analog equalization of a
5   data signal received over a data transmission channel
comprising a Master Delay Locked Loop (MDLL) for generat-
ing equidistant reference phase signals; a Slave Delay
Line (SDL) formed by serial connected Slave Delay Units
(SDU), wherein each Slave Delay Unit (SDU) has a Slave
10 Delay Element (SDE) to delay the received data signal
with a predetermined delay time (ΔT) and an analog ampli-
fier which amplifies the delayed output signal of the
Slave Delay Element (SDE) with a respective weighting co-
efficient to generate a weighted delay signal, wherein
15 the analog amplifier is switched transparent in response
to a corresponding reference phase signal generated by
said Master Delay Locked Loop (M-DLL); and subtracting
means for subtracting the weighted delay signals which
are selected by means of a multiplexer from the received
20 data signal to generate an equalized output data signal.

(Figure 5)

Reference List

	1	feed forward equalizer
	2	data input
5	3	transmitter
	4	data transmission channel
	5	data output
	6	decision unit
	7	clock input
10	8	clock signal generator
	9	control input
	10	control unit
	11	master delay locked loop
	12	slave delay line
15	13	slave delay unit
	14	control register
	15	control line
	16	reference signal line
	17	amplifier output line
20	18	multiplexer input
	19	multiplexer
	20	multiplexer output
	21	multiplexer control input
	22	multiplexer control input lines
25	23	multiplexer output lines
	24	substracting means
	25	input buffer
	26	input buffer
	27	post amplifier stage
30	28	master delay unit
	29	master delay element
	30	analog amplifier
	31	input buffer
	32	amplifier
35	33	phase detector

| 34 | low path filter |
| 35 | feedback line |